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1 **An adaptive CMOS transmission line driver**
Patel, H.N.; Hohl, J.H.; Oalusinski, O.A.;
ASIC Conference and Exhibit, 1993. Proceedings., Sixth Annual IEEE International , 27 Sept.-1 Oct. 1993
Pages:460 - 463

[Abstract] [PDF Full-Text (240 KB)] **IEEE CNF**

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2 **Package clock distribution design optimization for high-speed and low-power VLSIs**
Qing Zhu; Tam, S.;
Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on [see also Components, Hybrids, and Manufacturing Technology, IEEE Transactions on] , Volume: 20 , Issue: 1 , Feb. 1997
Pages:56 - 63

[Abstract] [PDF Full-Text (228 KB)] **IEEE JNL**

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3 **Embedded at-speed test probe**
Aigner, M.;
Test Conference, 1997. Proceedings., International , 1-6 Nov. 1997
Pages:932 - 937

[Abstract] [PDF Full-Text (448 KB)] **IEEE CNF**

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[PDF] PROGRAMMABLE **ASIC** I/O CELLS
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... **Transmission line** termination (a) Open-circuit or capacitive termination (b ... glitches (e) A typical FPGA input **buffer** with a ... of a logic gate or an **ASIC** (e) The ...
www.utdallas.edu/~zhoud/IOcells.PDF - Similar pages

UTD Electrical Engineering Course Descriptions
... and implementation of an **ASIC** digital signal ... reciprocity theory; basics of **transmission line** theory and ... implementation of logic, memory, **buffer**, and conversion ...
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6.2 AC Output
... The **ASIC** CHIP1 contains a bus keeper, BK1 ... that sense when the input to an output **buffer** changes ... this case we may have to consider the bus as a **transmission line**. ...
www-ee.eng.hawaii.edu/~msmith/ ASICs/HTML/Book2/CH06/CH06.2.htm - 30k - Cached - Similar pages

6.10 Problems
... TABLE 6.7 Programmable **ASIC** I/O logic resources (contd ... c) What difference does it make if the output **buffer** is complementary ... 6.11 (**Transmission line** bias, 10 min ...
www-ee.eng.hawaii.edu/~msmith/ ASICs/HTML/Book2/CH05/CH06.a.htm - 75k - Cached - Similar pages
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E*ECAD - Tools By Provider
... Integrated **ASIC** P&R interfaces are included; Full batch ... value selection and location, and **buffer** size selection ... **Transmission Line** and Package Modeling Solution. ...
www.eecad.com/site/tools_by_provider.php?company=4 - 48k - Cached - Similar pages

MTSC Moxa Technical Support Center
... **ASIC** chips can replace general-purpose commercial ... memory provides a large **buffer** that eliminates the ... resistance junctions in a **transmission line**, the impedance ...
www.moxa.com/support/glossary.htm - 59k - Cached - Similar pages

[PDF] "Output Jitter of CDC111/CDCVF111 in **ASIC** Networking Application"
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... In this **ASIC** event, both the CDC111/CDCVF111 ... The CDCVF111 clock **buffer** is characterized for ... the characteristic impedance (50 Ω) of the **transmission line**. ...
focus.ti.com/general/docs/lit/ getliterature.tsp?baseLiteratureNumber=scaa051 - Similar pages

Real World Technologies - Direct Rambus Memory, Part 1 - The ...
... provided by the memory controller **ASIC** to control ... signal both to prevent **transmission line** reflections and ... source Rambus signaling level (RSL) output **buffer**. ...
www.realworldtech.com/page. cfm?ArticleID=RWT110799000000&p=2 - 34k - Cached - Similar pages

FreeLists / si-list / [SI-LIST] Re: pci driver strength
... This can be derived from a **transmission line** by measuring the ... strength Hi, I am working on an **ASIC** that has ... I am doing hspice simulation on the output **buffer**. ...
www.freelists.org/archives/ si-list/08-2001/msg00019.html - 13k - Oct 24, 2004 - Cached - Similar pages

FreeLists / si-list / [SI-LIST] Re: SV: Total load capacitance
... means that the wire is not a wire, but a **transmission line**. ... is like a resistive load to the **buffer** with a ... determining the drive strenght needed for an **ASIC** I/O ...
www.freelists.org/archives/ si-list/01-2002/msg00091.html - 16k - Oct 24, 2004 - Cached - Similar pages
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[PDF] LVDS: Five tips for buffering signal integrity
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... Some **ASIC** and FPGA LVDS I/O may not be as suited ... Use a logic **buffer** to drive multiple loads and/or long ... bus may also need to be treated as a **transmission line**. ...
www.eetasia.com/ARTICLES/ 2001AUG/2001AUG09_RFD_EDA_TAC.PDF - Similar pages

[PDF] EET-ASIA/semicon temp
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... on I/O matching requirements (**ASIC**, memory, CPU ... circuits and load (such as **transmission line** balancing, cross ... contribution and input sensitivity of the **buffer**. ...
www.eetasia.com/ARTICLES/ 2003MAR/B/2003MAR16_NTEK_PD_TA.PDF - Similar pages
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